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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,918	11/14/2003	Mitsuyoshi Mori	60188-710	7667

7590 02/07/2006

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EXAMINER	
INGHAM, JOHN C	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,918	MORI ET AL.	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-10 and 12-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-10 and 12-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/13/04;5/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims **6, 18, and 28** recite the limitation "output transistor". There is insufficient antecedent basis for this limitation in the claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **3, 7-9, 12, 14, 26, 28, 31-34 and 36** are rejected under 35 U.S.C. 102(b) as being anticipated by Guidash (US 6,552,323).

4. Regarding claims **12 and 31**, Guidash discloses in Figure 2c a solid state imaging apparatus comprising: a plurality of photoelectric elements (PD1, PD2) arranged in an array of at least two rows and two columns (col 3 ln 60-63); a plurality of switching elements (gates connected to Rsel1, Rsel2), each of which is connected to one of said plurality of photoelectric elements, each of said switching elements operative for transferring charges from one of said photoelectric elements to one of a plurality of storage nodes (center node of Figure); a plurality of read lines including a first read line (Rsel1) coupled to one of two (i.e. a first) switching elements which are coupled to a first storage node, and a second read line (Rsel2) coupled to one of two

(i.e. a second) switching elements which are coupled to a second storage node (col 4 ln 18-21); and said first read line also coupled to one of said two switching elements coupled to said second storage node, said second read line also coupled to one of said two switching elements coupled to said first storage node (node shared by 30a and 30b in Fig 2c).

5. Regarding claim **14**, Guidash discloses the apparatus of claim 12 wherein the storage node is arranged between the two photoelectric elements, which are adjacent to each other in the row direction (col 2 ln 55-57).

6. With regards to claims **8 and 26**, Guidash discloses in Figure 6b the apparatus of claims 31 and 12, respectively, wherein the photoelectric elements are arranged so as to be spaced apart from each other by a certain distance in the row direction.

7. Regarding claim **28**, Guidash discloses in column 1, lines 40-43, that the apparatus comprises a signal processing circuit for processing an output signal.

8. Regarding claim **32**, Guidash discloses in Figure 2c the apparatus of claim 31, wherein upon activation of said first read line both of said switching elements coupled to said first read line are activated, wherein one of said switching elements transfers charge to the first storage node, and the other switching element transfers charge to the second storage node (see paragraph 12 below).

9. Regarding claim **33**, Guidash discloses in Figure 2c the apparatus of claim 32, wherein upon activation of said second read line both of said switching elements coupled to said second read line are activated, wherein one of said switching elements

transfers charge to the first storage node, and the other switching element transfers charge to the second storage node (see paragraph 10 below).

10. Regarding claim **9**, Guidash discloses in column 1, lines 40-43, that the apparatus of claim 33 further comprises a signal processing circuit for processing an output signal from said output transistor.

11. With regards to claim **36**, Guidash discloses in Figure 2c and column 1, lines 40-43 that the apparatus has a plurality of read lines connected to a vertical scanning circuit (x-y addressability).

12. Regarding claim **3**, Guidash discloses the apparatus of claim 35 wherein one switching element coupled to the first storage node (first column pair signal line) and one switching element coupled to the second storage node (second column pair signal line) are included in two adjacent columns (col 2 ln 59-60 and col 4 ln 23-25 recite that each pair of columns shares a signal line, or node). Four columns would include two signal lines, and adjacent columns 2 and 3 would have two different storage nodes.

13. With regards to claim **34**, Guidash discloses in column 2 lines 25-26 wherein the plurality of photoelectric elements are photo diodes.

14. Regarding claim **7**, Guidash discloses in Figure 2a a reset element (R_G) for resetting charge stored in the first storage node.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

17. Claims **2, 4-6, 13, 15-25, 35** are rejected under 35 U.S.C. 103(a) as being unpatentable over Guidash and Guidash (US 6,352,869), hereinafter patent '869.

18. Regarding claim **13**, Guidash discloses the apparatus of claim 12 but does not disclose a reset transistor for resetting charge stored in each storage node and an output transistor for detecting and outputting a voltage converted from the storage node, wherein a drain of the reset transistor is connected to a drain of the output transistor.

Patent '869 teaches a reset transistor (Fig 3b item R_G) for resetting charge stored in a storage node (FD) and an output transistor (Fig 3b item 32) for detecting and outputting the voltage, wherein the drain of the reset transistor (V_{DD}) is connected to the drain of the output transistor. It would have been obvious to one of ordinary skill in the art at the time of the invention to use to teachings of pate '869 on the structure of Guidash, in order to save space by sharing a reset transistor and output transistor between at least two photoelectric elements in the array (col 3 ln 35-40).

19. With regards to claim **15,** patent '869 discloses in Figure 3b wherein the switching transistor (T_G1b) is made of an MIS transistor, and a gate of the MIS is arranged in the row direction (Fig 3a).

20. Regarding claim **16**, patent '869 discloses in Figure 3a wherein said output transistor (32) is arranged between rows, which include some of the photoelectric elements adjacent to each other.

21. With regards to claim **17**, patent '869 discloses in Figure 3a the apparatus of claim 13 wherein the output transistor (32) and storage node (FD) are arranged between the first read line (T_G1a) and the second read line (T_G2a).

22. Regarding claim **18**, patent '869 discloses in Figure 3a the apparatus of claim 12, wherein the plurality of photoelectric elements arranged in an array of two columns defines a photoelectric section; and the output transistor (32) is arranged between the two photoelectric sections, which are adjacent to each other in the column direction.

23. Regarding claim **19**, patent '869 discloses in Figure 3a the apparatus of claim 15 wherein each output transistor (32) is arranged between the gate of a first MIS transistor (52) and the gate of a second MIS transistor (62).

24. With regards to claim **20**, patent '869 discloses in Figure 3a the apparatus of claim 13 wherein each said reset transistor (36) is arranged between the first read line (T_G1a) and the second read line (T_G2a).

25. Regarding claim **21,** patent '869 discloses in Figure 3a the apparatus of claim 18, wherein the output transistor (32) and the storage node (FD) are arranged between the two photoelectric sections, which are adjacent to each other.

26. Regarding claim **22**, patent '869 discloses in Figure 3a the apparatus of claim 18, wherein the reset transistor (36) is arranged between the two photoelectric sections, which are adjacent to each other in the row direction.

27. With regards to claim **23**, patent '869 discloses in Figure 3a the apparatus of claim 18 wherein the reset transistor (36) is arranged between the two photoelectric sections, which are adjacent to each other in the column direction.

28. With regards to claim **24**, patent '869 discloses in Figure 3a the apparatus of claim 15 wherein said reset transistor (37) is arranged between the gate of a first MIS transistor (52) and the gate of a second MIS transistor (62).

29. Regarding claim **25**, patent '869 discloses in Figure 3a the apparatus of claim 18, wherein the storage node (FD) is arranged between the two photoelectric sections that are adjacent to each other in the column direction.

30. Regarding claim **35,** patent '869 discloses the apparatus of claim 31, further comprising: an output transistor which is coupled to the first storage node; and the output transistor comprises of a source follower transistor which detects and outputs a voltage potential converted from said first storage node.

31. With regards to claim **4**, patent '869 discloses in Figure 3b the apparatus of claim 35, wherein each storage node (FD) and each said output transistor (32) are shared by the two switching elements (T_G1, T_G2) which are coupled to the first and the second read line respectively.

32. Regarding claim **5**, patent '869 discloses in Figure 3b the apparatus of claim 35, further comprising: a signal line (87) for outputting a signal from the output transistor

(32) to the outside; and a select transistor (34) which is provided between the output transistor and the signal line.

33. Regarding claim **6**, patent '869 discloses in Figure 3b the apparatus of claim 34 wherein the first storage node (FD) and the output transistor (32) are shared by photoelectric elements (PD1a, PD2a), which are adjacent to each other in the row direction (Fig 3a).

34. Regarding claim **2**, patent '869 discloses in Figure 3bthe apparatus of claim 31, wherein one element coupled to the first storage node (FD) and one element coupled to the second storage node are included in the same column (a unit cell is shown in the Figure, the next row of pixel sections will include an element in column 1 that is connected to a second node).

35. Claims **29 and 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Guidash as applied to claim 31 above, and further in view of Patterson (US 6,541,794).

Guidash discloses each limitation as claimed in claims 29 and 30 (see paragraph 4 above) except for disclosing that the solid state imaging apparatus is part of a camera. Patterson teaches that arrays of photoactive pixel circuits are used in cameras (col 1 ln 11) since they are suitable for capturing images projected onto the arrays (col 1 ln 7). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Patterson on the array disclosed by Guidash in order to capture images.

36. Claims **10 and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Guidash as applied to claim 31 above, Patent '869, and further in view of Yamazaki (US 2002/0145582).

Guidash discloses each limitation as claimed in claim 31 (see paragraph 4 above). Patent '869 shows that the plurality of photoelectric elements arranged in an array of at least two rows and two columns define a unit of a photoelectric section (Fig 3a). Neither one teaches that the sections are separated from one another by a power supply line which also functions as a light-shielding film, or that the shared line (V_{DD}) of the reset transistor and output transistor functions as a light-shielding film.

Yamazaki teaches the use of a power supply line between pixels (or sections), which is also used as a light shield in order to protect the channel formation regions and p type semiconductor regions (¶ 90). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Yamazaki on the structure of Guidash and patent '869 to use the power supply line as a light shield for channel and p type regions between pixels and/or pixel sections. Since V_{DD} is a power supply line, it follows that the shared line of the reset transistor and output transistor would also be used as a light shield.

Conclusion

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Takahashi (US 5,955,753) discloses a circuit arrangement in Figure 1 that shares storage nodes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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jci

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PRIMARY EXAMINER